

Characterizing the Noise Performance of the *KPiX* ASIC Readout Chip

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ABSTRACT

Characterizing the Noise Performance of the *KPiX* ASIC Readout Chip. JEROME KYRIAS CARMAN (Cabrillo College, Aptos, CA 95062) TIMOTHY KNIGHT NELSON (Stanford Linear Accelerator Center, Stanford, CA 94025)

KPiX is a prototype front-end readout chip designed for the Silicon Detector Design Concept for the International Linear Collider (ILC). It is targeted at readout of the outer tracker and the silicon-tungsten calorimeter and is under consideration for the hadronic calorimeter and muon systems. This chip takes advantage of the ILC timing structure by implementing pulsed-power operation to reduce power and cooling requirements and buffered readout to minimize material. Successful implementation of this chip requires optimal noise performance, of which there are two measures. The first is the noise on the output signal, previously measured at $1500e^-$, which is much larger than the anticipated $500e^-$. The other is the noise on the trigger logic branch, which determines where thresholds must be set in order to eliminate noise hits, thus defining the smallest signals to which the chip can be sensitive. A test procedure has been developed to measure the noise in the trigger branch by scanning across the pedestal in trigger threshold and taking self-triggered data to measure the accept rate at each threshold. This technique measures the integral of the pedestal shape. Shifts in the pedestal mean from injection of known calibration charges are used to normalize the distribution in units of charge. The shape of the pedestal is fit well by a Gaussian, the width of which is determined to be $2480e^-$, far in excess of the expected noise. The variation of the noise as a function of several key parameters was studied, but no significant source has been clearly isolated. However, several problems have been identified that are being addressed or are under further investigation. Meanwhile, the techniques developed here will be critical in ultimately verifying the performance goals of the *KPiX* chip.

INTRODUCTION

The proposed International Linear Collider (ILC), in contrast to the Large Hadron Collider (LHC), presents a benign environment for detector components since e^+e^- collisions produce events with relatively few background processes resulting in a much lower data rate and a mild radiation environment. This feature allows for the study of many processes that are buried underneath vast amounts of data produced in hadronic collisions, enabling detailed investigations of the Higgs sector and any new physics such as supersymmetry or extra dimensions that may be revealed by the LHC. While this optimal environment, combined with the high energies of ILC, presents an enticing opportunity for the study of rare high energy physics events, delivering on this promise presents numerous detector design challenges. In particular, detector performance requirements include precise momentum resolution for charged tracks and successful implementation of the “particle flow” calorimetry concept[1] via a highly granular calorimeter design.

Currently there are four proposed detector designs[1], one of which is referred to as the Silicon Detector (SiD) Concept. This concept utilizes all-silicon tracking, a silicon-tungsten electromagnetic calorimeter, and a single 5T solenoid (see Figure 1). A silicon sensor readout chip called *KPiX* is currently being developed for use in the outer tracker and the silicon-tungsten calorimeter. This device is also being considered for use in the hadronic calorimeter and the muon system. *KPiX* utilizes a number of state-of-the-art ideas to accommodate ILC physics requirements.

A key feature of the ILC is that e^- and e^+ beams are delivered in 1ms “trains” consisting of 2652 particle bunches, with each bunch separated by 369ns. These trains are repeated at a rate of 5Hz providing 199ms of quiet time between trains. This feature allows a “pulsed power” [2] concept which only runs the analog components of the *KPiX* chip during each train. Successful implementation of pulsed power operation reduces power consumption

by two orders of magnitude compared with continuous readout. This allows a simpler air cooled design and significant material reduction in comparison to liquid cooled detectors. Meanwhile, the low cross-section for e^+e^- collisions at the ILC results in very low per-channel occupancies in the outer detectors. Therefore, a small number of readout buffers per channel are capable of holding all data generated by all collisions in each bunch train. Implementation of buffered readout in *KPiX* via storage of signals in four bunch-tagged analog buffers followed by digitization and readout between trains results in further simplification. This is because lack of noise from digitization and readout during the trains allows the chip to be bump-bonded directly to the face of an active sensor, eliminating additional material usually required to isolate the sensor from the readout chip.

The *KPiX* chip is in an early prototyping phase and much testing and debugging remains [2] in order to understand its behavior and refine the design to achieve optimal performance. This paper presents an analysis of the analog front end of prototype version 4 of the *KPiX* chip. There are many features which work in concert to balance the need for high bandwidth during acquisition with the requirement of low noise occupancy in the storage buffers. In particular, the threshold trigger logic is critical to this task as it is responsible for selecting signals and rejecting noise. The studies presented characterize the noise in the trigger branch through a carefully designed test procedure and attempt to isolate noise sources by studying its dependence on key parameters.

MATERIALS AND METHODS

The KPiX Chip

KPiX is a multi-channel readout chip designed to amplify, shape, buffer, and digitize input signals from a silicon sensor. Each individual channel consists of an analog block connected to a digital block, both of which communicate through an address register block. The main

components of the analog section consist of a transconductance amplifier, a signal pulse shaper, reset and trigger logic, and four capacitive storage buffers. In the digital section, the signals in the analog buffers are converted to digital values via a Wilkinson analog-to-digital converter (ADC) and are read out through differential low-voltage digital signal lines. The trigger branch, which decides which events to store in the buffers, is of particular interest here as it must be optimized to provide high efficiency for real signals while minimizing the probability of storing noise hits throughout an entire bunch train. Since the expected event signals are quite small, typically $22,000e^-$, and may be distributed across two or more channels, the noise at the trigger stage must be low in order to efficiently select them without storing random noise during the long (1ms) acquisition cycle.

In order to accurately calibrate the *KPiX* chip a set of four 200fF calibration capacitors are integrated on-chip to inject signals of known charge. A digital-to-analog converter (DAC) applies a known voltage to these capacitors according to a digital input value, therefore storing a known charge which is placed on the input of a specified channel at a specified time. This feature is crucial for calibrating the charge corresponding to both an output ADC count and a trigger threshold DAC step.

To minimize charge buildup within the analog circuitry the *KPiX* includes a periodic channel reset. The threshold trigger logic consists of a pre-trigger discriminator designed to delay the onset of the channel reset in order to allow the pulse shaper enough time to build a possible signal. Since a reduced shaper bandwidth generally results in an improved signal-to-noise ratio (S/N), the pre-trigger attempts to balance a high acquisition rate with a long integration time. In practice the pre-trigger threshold value should be set somewhere between the noise pedestal and the trigger threshold. If a signal reaches the pre-trigger threshold value, channel reset is delayed and the signal is given a chance to reach the trigger threshold value, in which case the signal is stored.

The charge amplifier of the *KPiX* chip can amplify a signal via three different gain

modes. Low gain utilizes a 10pF feedback capacitor, normal gain a 400fF feedback capacitor, and double gain a pair of 400fF capacitors. The intention is to use normal gain to allow sufficient amplification of low charge signals from minimum ionizing particles (MIPs), with logic included to automatically switch to low gain when the signal is large enough to approach ADC saturation as will be the case for large showers in the silicon-tungsten calorimeter. Double-gain mode reduces noise due to reference voltage fluctuations on the chip for best performance with small signals, as will be the case in the tracker. An additional amplifier is included which, when enabled, inverts the voltage polarity of the inputs. The purpose of this is to allow for readout of different types of sensors, such as the gas electron multipliers (GEMs) being considered for the SiD HCal. This amplifier also features twice the gain of the normal gain mode of the primary amplifier.

In all tests a silicon sensor is wire-bonded to the *KPiX* chip which is attached to a daughter board (see Figure 2) connected to version 2 of a *KPiX* test board. This test board is connected via USB to a computer from which various programs are used to operate the chip and process the data collected. The *KPiX* chip, daughter board and test board are located inside an aluminum box which both acts as a Faraday cage and keeps the sensor optically isolated. Analog and digital voltages (AVDD and DVDD) are both set at 2.5V which is provided by regulators operating from an external Power Designs TP340 power supply set at 7.5V. Eight 9V batteries supply a noise-free 72V bias to the silicon strip sensor.

Analysis Software

A program called `thresh_scan` was developed to scan *KPiX* over a range of trigger and pre-trigger threshold values to allow the measurement of the trigger accept rate at each threshold. Data is taken without calibration charge injected in order to measure the bare pedestal, and with various calibration pulses of known charge in order to establish the charge equivalence of the threshold values. Calibration pulses are chosen to be close to the upper tail of the bare

pedestal to minimize uncertainties due to possible non-linearities in the calibration pulses or threshold settings. All tests look at a single channel, usually channel 0, since the *KPiX* bus traces leading to this channel are the least likely to be susceptible to cross talk from other channels because of their physical location.

This program utilizes the timing sequence shown in Figure 3 by repeating the sequence numerous times at each threshold to minimize statistical errors. The two significant bunch crossing times referred to in most tests are shown; bunch crossing 1254 and 2564. These times correlate to a delay of four bunch crossings after the threshold trigger logic enable time of 1250 where the bare pedestal is measured, and a delay of four bunch crossings after the calibration strobe injection time of 2560. The delay between action and sample time is expected and these choices of bunch number are largely arbitrary.

A number of programs were developed to analyze the data generated by the `thresh_scan` program. The `thresh_scan_plot` program is used to observe the general location of the noise and calibration pulse pedestals in threshold DAC steps. The `thresh_stime_hist` program is used to display a histogram of trigger times which spans the length of a single bunch train to help identify the correct timing for the threshold scan. The recorded samples are plotted with respect to the specific bunch crossing at which they occur. Figure 4 shows an example.

The key piece of analysis software is the `thresh_stime_plot` program which plots the accept rate of the trigger as a function of threshold. For the bare pedestal, the rate at which samples appear in the first buffer at time 1254 is plotted as a function of threshold. The resulting s-shaped curve is the integral of the bare pedestal, the width of which is a measurement of the critical noise in the trigger branch. This plot is divided by the total number of samples taken at each threshold in order to calculate the fraction of the pedestal that lies above a given threshold. The errors on these fractions are calculated according to Bayesian binomial errors which are asymmetric near zero and one. Errors associated with threshold DAC values are set to zero as these are discrete voltage values and ideally have

no uncertainty. Using the MINUIT fitting package, the Gaussian cumulative distribution function is fitted to the data to extract the associated mean and one-standard-deviation errors. To express the noise in terms of equivalent noise charge (ENC) the plot at bunch crossing 2564 is considered for multiple calibration charges. The relative shift in the mean value of the resulting s-curves correspond to a single DAC step in the calibration pulse (see Figure 5). Since the charge of a calibration pulse is known, a plot of the mean threshold value as a function of charge can be made (see Figure 8), the slope of which is used to convert threshold DAC steps into units of charge.

To compare the noise at the trigger branch with that from the ADC, the `calib_dist` program is used. Noise is measured by repetitively injecting the same calibration pulse voltage and force triggering the chip to store the resulting distribution, the width of which measures the noise. The ADC gain is measured by injecting a range of known calibration pulses. The `calib_dist_plot` program utilizes this data to plot the ADC gain as function ADC counts versus charge. The noise is plotted as the distribution of samples versus ADC counts.

RESULTS

The noise of the bare pedestal and the threshold DAC gain are measured in normal gain mode with the pre-trigger function disabled by setting it equal to the trigger threshold at each step. The Gaussian cumulative distribution function fits the data well as shown in Figure 6. Taken together with the threshold gain in DAC/fC shown in Figure 8, the one-sigma noise is $2480e^-$ as summarized in Table 1. For comparison, the noise at the ADC is estimated to be $1500e^-$ from the forced-trigger distribution shown in Figure 7, with ADC counts converted to charge using the gain curve of Figure 9. All results are for channel 0, but are typical for other channels.

These measurements are repeated in several different configurations in an attempt to understand the noise sources as summarized in Table 1. First, the noise is measured with the inverted amplifier enabled to compare the noise when the gain of the amplifier is doubled. This results in a noise measurement of $4680e^-$. Second, the noise is measured with the channel reset disabled, since recent literature suggests that a periodic reset may be a significant noise source in such designs [3]. The periodic reset is disabled by setting the pre-trigger threshold significantly below the bare pedestal. The threshold trigger enable time is decreased to bunch crossing 50 and the calibration strobe is injected at bunch crossing 56 to avoid charge buildup due to lack of reset from affecting the results. The magnitude of the measured noise reveals a slight relative increase to 1.056 threshold DAC steps. However, this result is somewhat inconclusive since the chip refused to trigger on the calibration pulses and the measurement of threshold gain could not be verified. The reason for this is not known.

An additional experiment looks at the affect of lowering the analog and digital voltage from 2.5V to 1.8V. A different *KPiX* chip, running at lower voltage and without an attached sensor, was used and found to have a noise of $1170e^-$ as shown in Table 1. The sensor, with a capacitance of less than 10 pF, should not significantly change the chip behavior, but results are inconclusive since this chip was found to be damaged while attempting to run at 2.5V as a cross-check.

Another test investigates a longer shaper differentiation time, which is accomplished by changing the shaper bias with a $100M\Omega$ resistor on the test board. This test resulted in very similar noise behavior, as shown in Table 1. However, the measured gain, which should have changed significantly due to this modification, remained the same contrary to expectation.

DISCUSSION AND CONCLUSIONS

The expected noise from the ADC for the configuration under test is less than $500e^-$ and the noise in the trigger branch should be similar. While the $1500e^-$ noise measurement from the ADC motivated the investigation of the trigger branch, the fact that the noise there is much larger still, $2480e^-$, is surprising since it was thought that the ADC itself was responsible. Instead, it appears there is at least one unexpected source of noise. Since uncorrelated noise adds in quadrature, these sources dominate the overall noise performance. The first significant result is therefore the fact that the shape of the pedestal is accurately represented by a Gaussian distribution, indicating that these unknown sources are random rather than systematic.

One possibility that would affect both the ADC output and the trigger branch is that the noise performance of the front-end amplifier driving both is much worse than expected. In this case, the factor-of-two gain change from operating in inverted mode would not alter the noise measurement. Another possibility is that there are fluctuations in the voltage references for the trigger threshold and the Wilkinson ADC, which would reduce the apparent noise in electrons by a factor of two in inverted mode. Thus, the result showing that the noise in inverted mode is larger, $4680e^-$, is puzzling and may indicate an additional problem with the inverted amplifier. Another method for performing this test was attempted utilizing the double gain feature of the primary amplifier to eliminate the inverter from the signal path. However, the double gain feature proved to be unstable in the current *KPiX* version. This test is a clear priority for future revisions of the chip.

Analysis of the affect of the periodic channel reset was inconclusive. While the noise measurement of 1.056 threshold DAC steps is similar and therefore inspires confidence in the channel reset design, the lack of a successful calibration measurement casts doubt on this result, since the chip was not designed to be operated in this mode. Further investigation is

required to understand the underlying cause of this behavior and fully eliminate the periodic reset as a noise source.

Interestingly, results of the AVDD and DVDD voltage settings of 1.8V, in addition to the different shaper bias results, while both inconclusive, may indicate issues with the pulse shaper. Given the significant role of the shaper in determining the performance of the trigger branch, development of additional tests to isolate shaper characteristics may well lead to answers to some of the questions raised here. Meanwhile, significant revisions to the operation of the shaper are being planned to eliminate possible issues that may relate to these observations.

Results of this project indicate that the noise performance of the trigger branch of the current *KPiX* prototype is insufficient for its primary mission in readout of the Si-W calorimeter and outer tracker of the SiD detector, since it will not be possible to trigger on minimum ionizing signals from the silicon sensors without accepting noise hits at a rate that will fill the readout buffers. This is a key result and indicates the need to further study the problem until a solution is found. Additional tests have established no clear evidence of noise produced by any of the expected sources, so an explanation of the characteristic noise of $2500e^-$ remains unresolved. Comparisons with data taken on a similar test setup at the University of Oregon have been generally consistent when analyzed with these methods. It is anticipated that the techniques developed here will be vital in continued efforts to isolate these issues and to establish that adequate performance has been achieved by future revisions of the *KPiX* chip, the next generation of which is currently in production.

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FIGURES

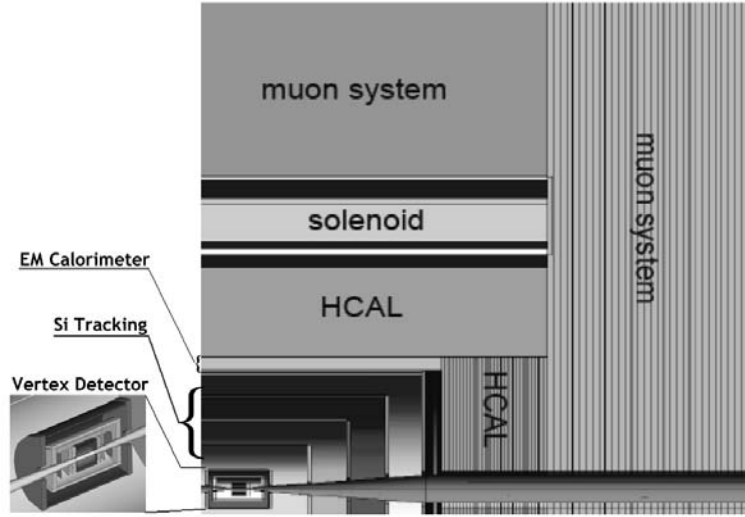


Figure 1: Cross section of the SiD detector design. Use of the *KPiX* chip for readout is planned or under consideration for every detector component shown except for the vertex detector.

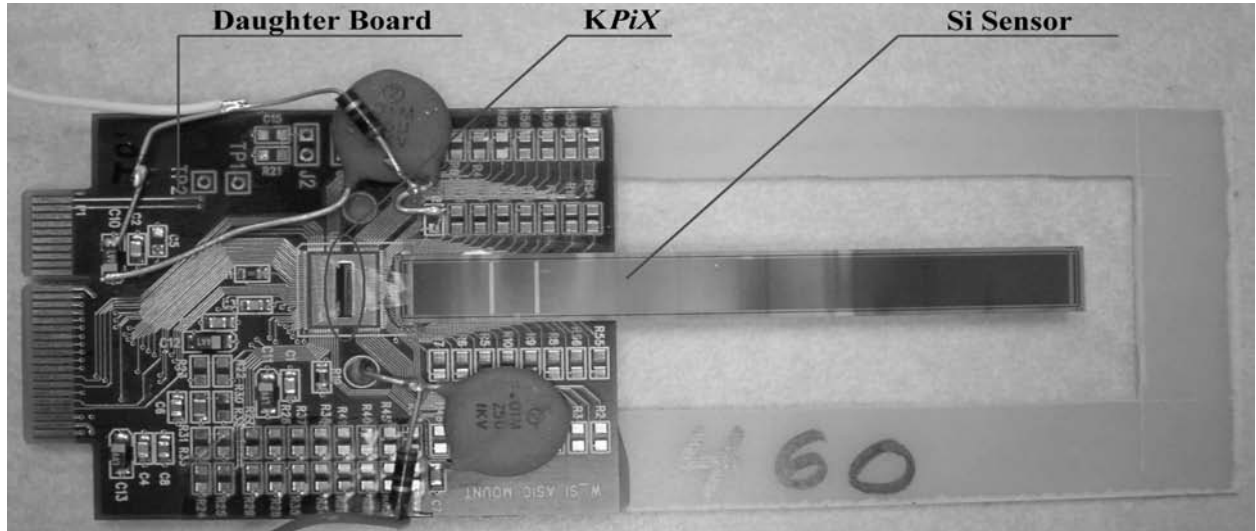


Figure 2: Image of a 64-channel *KPiX* mounted to a daughter board and wire-bonded to a spare silicon microstrip sensor from CDF Layer 00.

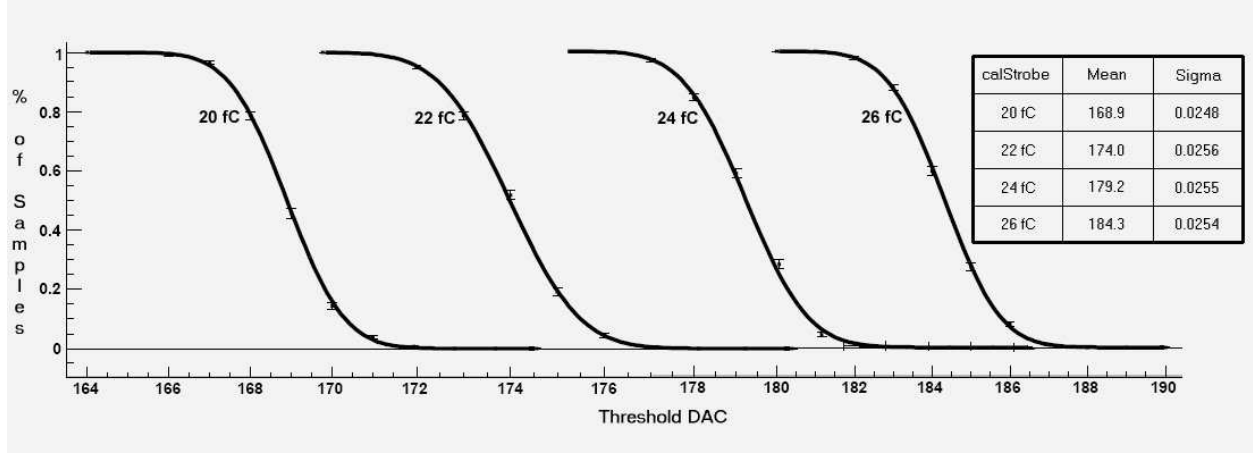


Figure 5: Plot of pedestal shifts in threshold with increasing calibration charge. The shifts are used to calibrate the charge corresponding to a threshold DAC step.

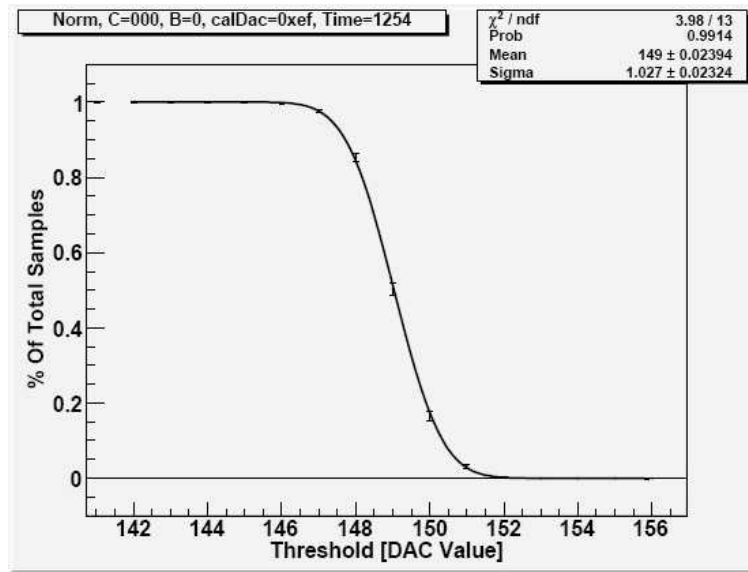


Figure 6: Noise measurement in threshold DAC steps at the trigger threshold logic in positive polarity mode for channel 0. Sigma is the one standard deviation noise, and the mean is the mean value of the pedestal.

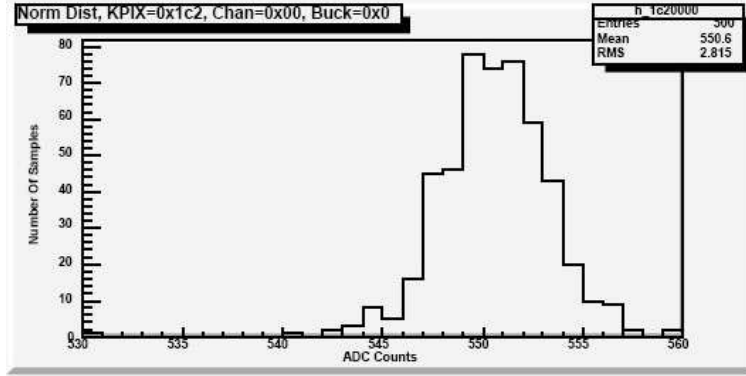


Figure 7: Noise measurement in ADC counts at the ADC for positive polarity mode for channel 0. RMS value is the one standard deviation noise, and the mean is the mean value of the pedestal.

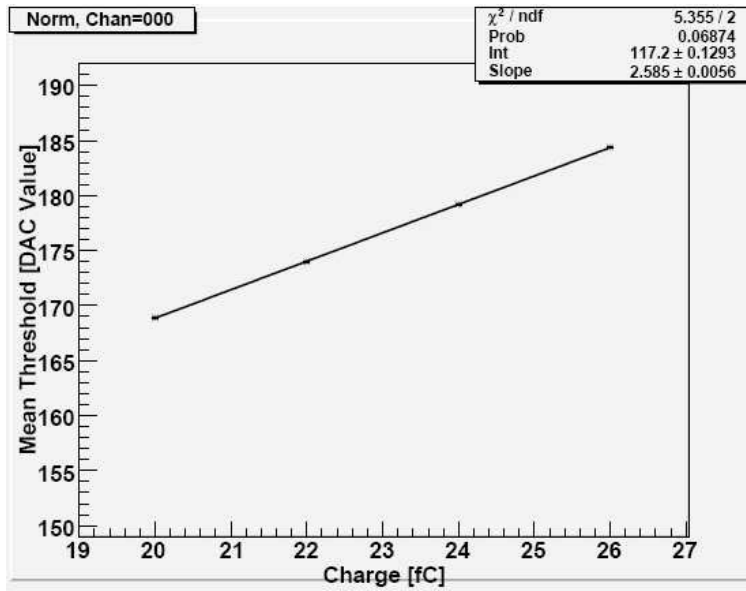


Figure 8: Results of a threshold DAC calibration test. The slope is the conversion factor from threshold DAC counts to calibration DAC counts, which are of known charge.

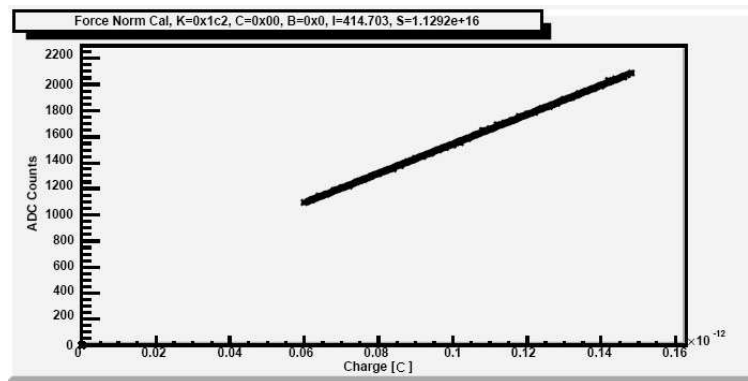


Figure 9: Results of an ADC count calibration test. The slope is the conversion factor from ADC counts to calibration DAC counts, which are of known charge.

TABLES

Experiment	1σ [DAC]	Gain [DAC/fC]	Noise [e^-]
Baseline Measurement	1.027 ± 0.023	2.585 ± 0.006	2480 ± 55.8
Inverted Amplifier	2.919 ± 0.039	3.894 ± 0.008	4680 ± 63.2
Periodic Reset	1.056 ± 0.036	Not Measured	≈ 2500 (using gain of 2.585)
1.8V AVDD and DVDD	0.610 ± 0.024	3.242 ± 0.008	1170 ± 46.3
100M Ω Shaper Bias	1.102 ± 0.120	2.528 ± 0.047	2720 ± 301

Table 1: Summary of noise and gain results at the trigger branch.